Radar FMCW estilo Nestransverter

Parte 0

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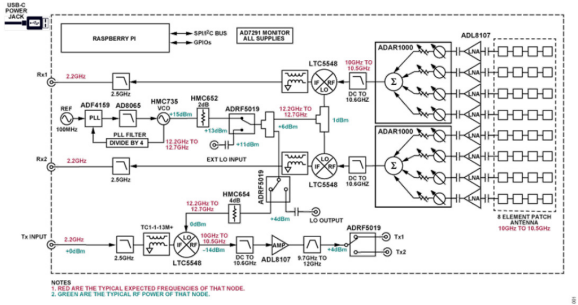
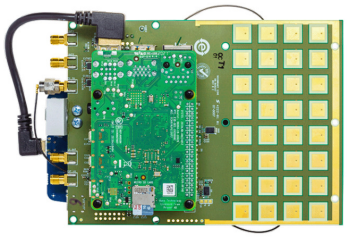
Micromeet 2026, Guadarrama

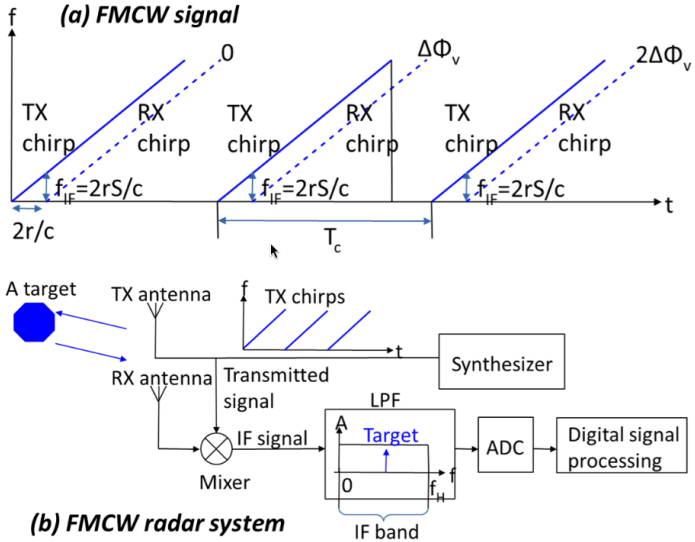
El año pasado...

ADALM-PHASER. https://www.analog.com/en/resources/reference-designs/circuits-from-the-lab/cn0566.html

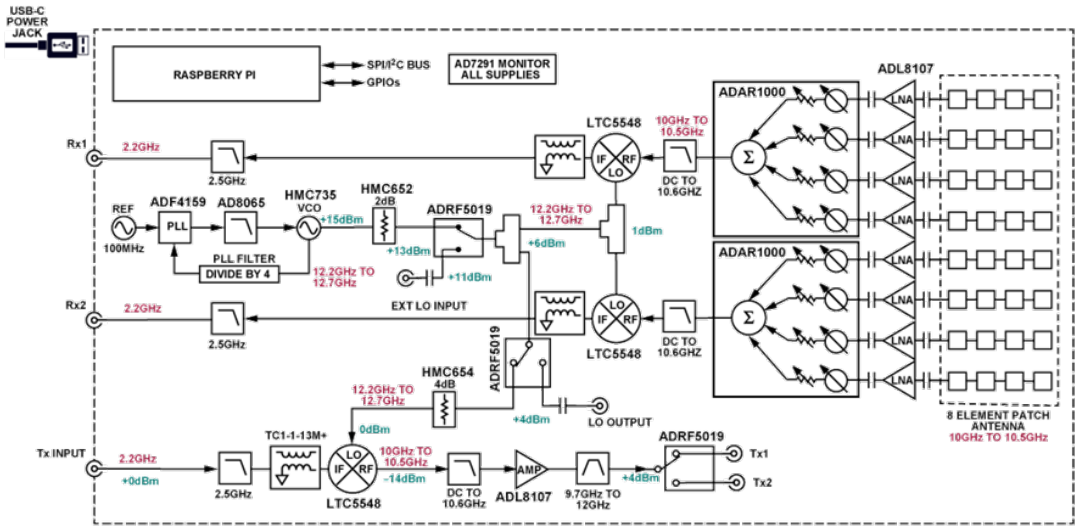




Introducción al radar FMCW

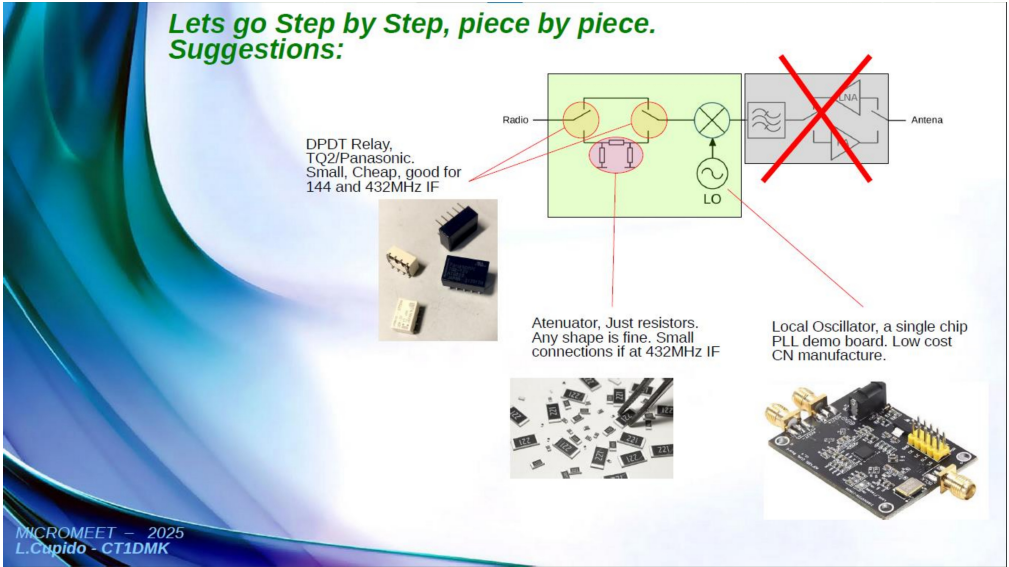


El ADALM-PHASER más en detalle



NOTES
1. RED ARE THE TYPICAL EXPECTED FREQUENCIES OF THAT NODE.
2. GREEN ARE THE TYPICAL RF POWER OF THAT NODE.

Diagrama de bloques del Nestransverter



Planificación de frecuencias

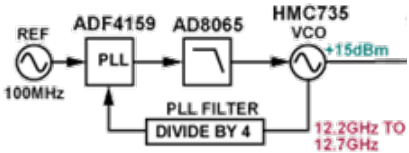
Nestransverter original (transverter para 10.368 GHz):

- LO 2.556 GHZ (ADF4351)
- Doblador LO 5.112 GHz
- IF 144 MHz
- Mixer armónico: $2 \times 5.112\ \mathrm{GHz} + 144\ \mathrm{MHz} = 10.368\ \mathrm{GHz}$

Radar FMCW 10 - 10.5 GHz:

- LO 4.2 - 4.45 GHz
- IF 1.6 GHz (no es crítico: podría ser cualquier cosa entre 1 y 3 GHz)
- Mixer armónico: $2 \times [4.2, 4.45]\ \mathrm{GHz} + 1.6\ \mathrm{GHz} = [10, 10.5]\ \mathrm{GHz}$

Selección de componentes

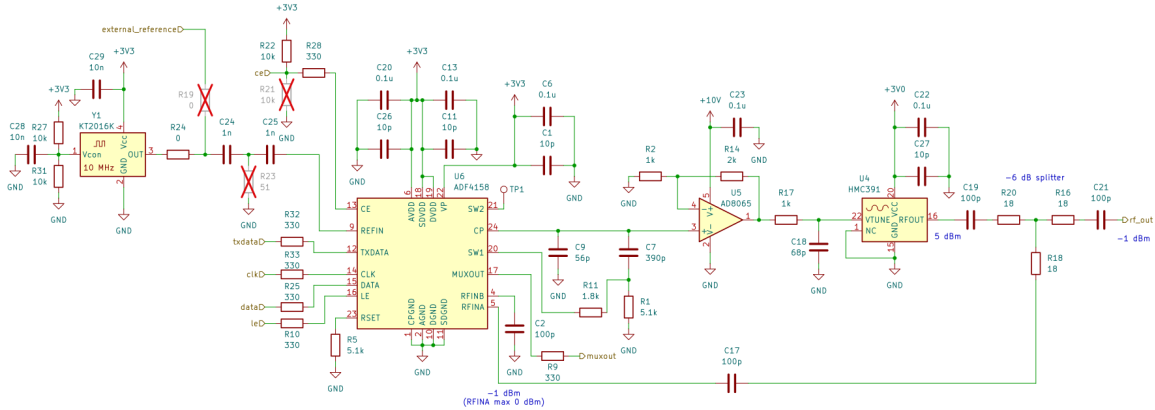


ADALM-PHASER:

- ADF4159: sintetizador hasta 13 GHz, 19€
- HMC735: VCO 10.5-12.2 GHz (con salida /4), 17 dBm, 56€
- AD8065: opamp 145 MHz, single supply, rail-to-rail, low noise, 5€

Mi radar:

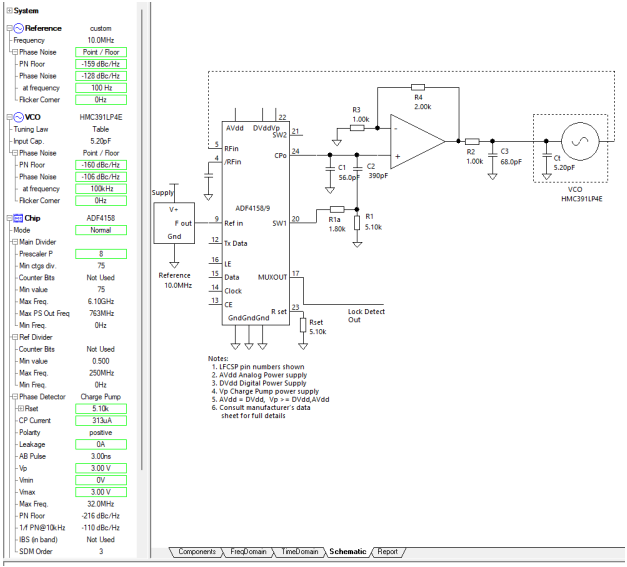
- ADF4158: sintetizador hasta 6.1 GHz, 13€
- HMC319: VCO 3.9-4.45 GHz, 5 dBm, 19€
- AD8065: coincidencia. El más razonable en la librería de ADIsimPLL

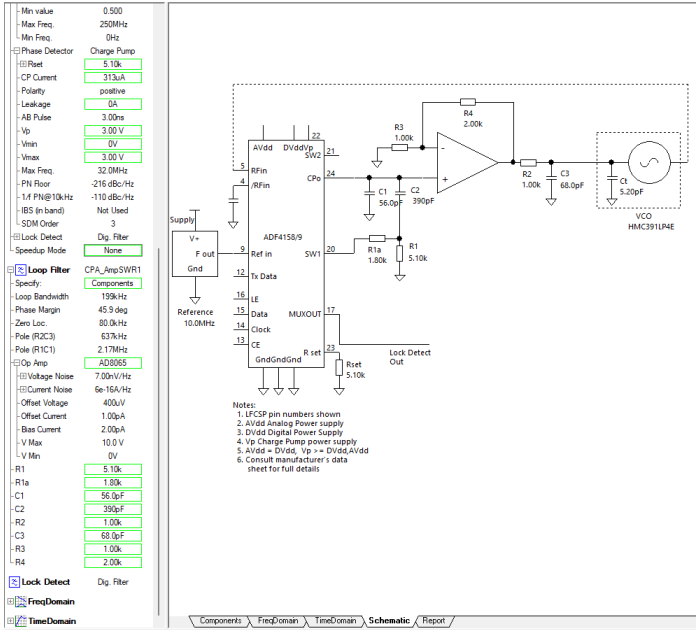

external_reference
+3V3
C29
10n
Y1
KT2016K
10 MHz
Vcon
GND
OUT
Vcc
C28
10n
R27
10k
R31
10k
R19
0
R24
0
C24
1n
R22
10k
R28
330
ce
R21
10k
C25
1n
R23
51
C20
0.1u
C26
10p
C13
0.1u
C11
10p
U6
ADF4158
CE
REFIN
TXDATA
CLK
DATA
LE
RSET
AVDD
DVDD
VVDD
VP
SW2
CP
SW1
MUXOUT
RFINB
RFINA
CPGND
AGND
DGND
SDGND
TP1
C6
0.1u
C1
10p
R32
330
R33
330
R25
330
R10
330
R5
5.1k
txdata
clk
data
le
C9
56p
C7
390p
R11
1.8k
R1
5.1k
C2
100p
R9
330
muxout
C17
100p
−1 dBm
(RFINA max 0 dBm)
R2
1k
+10V
C23
0.1u
R14
2k
U5
AD8065
R17
1k
C18
68p
+3V0
C22
0.1u
C27
10p
U4
HMC391
VTUNE
NC
GND
RFOUT
5 dBm
C19
100p
−6 dB splitter
R20
18
R16
18
C21
100p
rf_out
−1 dBm
R18
18

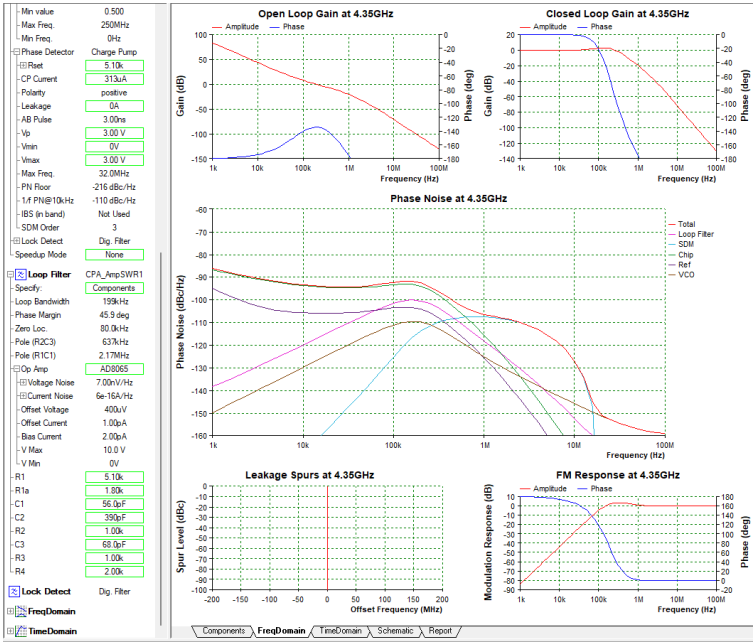
Diseño del waveform

- Parámetros: ancho de banda $B = 500\ \mathrm{MHz}$, periodo de chirp T, frecuencia de portadora $f_c = 10.25\ \mathrm{GHz}$.
- Resolución de distancia $\approx c/(2B) = 0.3\ \mathrm{m}$.
- Ambiguedad de Doppler $|f_d| \leq 1/(2T)$. Para $v = 250\ \mathrm{m/s}$ (900 km/h), el Doppler es $f_d = f_c v/c = 8.5\ \mathrm{kHz}$, así que tenemos $T \leq 60\ \mu\mathrm{s}$.
- Distancia máxima $\approx cT/4$ (50% superposición en chirp TX y RX). Esto es 4.5 km con $T = 60\ \mu\mathrm{s}$.
- Nota: con un SDR con ancho de banda B_{SDR} solamente podemos observar simultáneamente un rango de distancias de $cTB_{\mathrm{SDR}}/(2B)$. Con $B = 61.44\ \mathrm{Msps}$, tenemos 1.1 km de rango simultáneo.

Diseño del filtro del PLL: ADIsimPLL




Min value 0.500
Max Freq. 250MHz
Min Freq. 0Hz
Phase Detector Charge Pump
Rset 5.10k
CP Current 313uA
Polarity positive
Leakage 0A
AB Pulse 3.00ns
Vp 3.00 V
Vmin 0V
Vmax 3.00 V
Max Freq. 32.0MHz
PN Floor -216 dBc/Hz
1/f PN@10kHz -110 dBc/Hz
IBS (in band) Not Used
SDM Order 3
Lock Detect Dig. Filter
Speedup Mode None
Loop Filter CPA_AmpSWR1
Specify: Components
Loop Bandwidth 199kHz
Phase Margin 45.9 deg
Zero Loc. 80.0kHz
Pole (R2C3) 637kHz
Pole (R1C1) 2.17MHz
Op Amp AD8065
Voltage Noise 7.00nV/Hz
Current Noise 6e-16A/Hz
Offset Voltage 400uV
Offset Current 1.00pA
Bias Current 2.00pA
V Max 10.0 V
V Min 0V
R1 5.10k
R1a 1.80k
C1 56.0pF
C2 390pF
R2 1.00k
C3 68.0pF
R3 1.00k
R4 2.00k
Lock Detect Dig. Filter
FreqDomain
TimeDomain
AVdd
DVddVp
SW2
RFin
/RFin
CPo
ADF4158/9
Ref in
SW1
Tx Data
LE
Data
MUXOUT
Clock
CE
R set
GndGndGnd
Supply
V+
F out
Gnd
Reference
10.0MHz
Rset
5.10k
Lock Detect
Out
C4
5.20pF
VCO
HMC391LP4E
Notes:
1. LFCSP pin numbers shown
2. AVdd Analog Power supply
3. DVdd Digital Power Supply
4. Vp Charge Pump power supply
5. AVdd = DVdd, Vp >= DVdd.AVdd
6. Consult manufacturer's data sheet for full details
Components
FreqDomain
TimeDomain
Schematic
Report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Rset 5.10k
CP Current 313uA
Polarity positive
Leakage 0A
AB Pulse 3.00ns
Vp 3.00 V
Vmin 0V
Vmax 3.00 V
Max Freq. 32.0MHz
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Speedup Mode None
Loop Filter CPA_AmpSWR1
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Zero Loc. 80.0kHz
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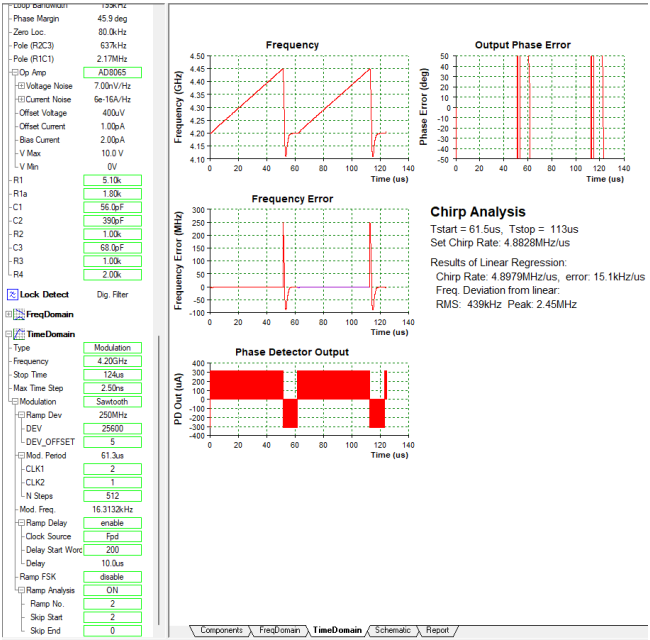
Current Noise 6e-16A/Hz
Offset Voltage 400uV
Offset Current 1.00pA
Bias Current 2.00pA
V Max 10.0 V
V Min 0V
R1 5.10k
R1a 1.80k
C1 56.0pF
C2 390pF
R2 1.00k
C3 68.0pF
R3 1.00k
R4 2.00k
Lock Detect Dig. Filter
FreqDomain
TimeDomain
Open Loop Gain at 4.35GHz
Amplitude
Phase
Gain (dB)
Phase (deg)
Frequency (Hz)
Closed Loop Gain at 4.35GHz
Amplitude
Phase
Gain (dB)
Phase (deg)
Frequency (Hz)
Phase Noise at 4.35GHz
Total
Loop Filter
SDM
Chip
Ref
VCO
Phase Noise (dBc/Hz)
Frequency (Hz)
Leakage Spurs at 4.35GHz
Spur Level (dBc)
Offset Frequency (MHz)
FM Response at 4.35GHz
Amplitude
Phase
Modulation Response (dB)
Phase (deg)
Frequency (Hz)
Components
FreqDomain
TimeDomain
Schematic
Report

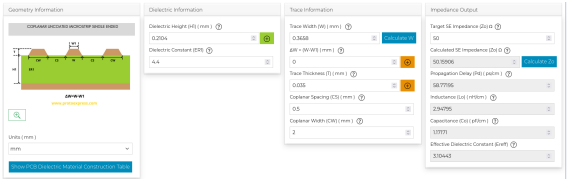

Loop Bandwidth 135kHz
Phase Margin 45.9 deg
Zero Loc. 80.0kHz
Pole (R2C3) 637kHz
Pole (R1C1) 2.17MHz
Op Amp AD8065
Voltage Noise 7.00nV/Hz
Current Noise 6e-16A/Hz
Offset Voltage 400uV
Offset Current 1.00pA
Bias Current 2.00pA
V Max 10.0 V
V Min 0V
R1 5.10k
R1a 1.80k
C1 56.0pF
C2 390pF
R2 1.00k
C3 68.0pF
R3 1.00k
R4 2.00k
Lock Detect
Dig. Filter
FreqDomain
TimeDomain
Type Modulation
Frequency 4.20GHz
Stop Time 124us
Max Time Step 2.50ns
Modulation Sawtooth
Ramp Dev 250MHz
DEV 25600
DEV_OFFSET 5
Mod. Period 61.3us
CLK1 2
CLK2 1
N Steps 512
Mod. Freq. 16.3132kHz
Ramp Delay enable
Clock Source Fpd
Delay Start Word 200
Delay 10.0us
Ramp FSK disable
Ramp Analysis ON
Ramp No. 2
Skip Start 2
Skip End 0
Frequency
Frequency (GHz)
Time (us)
Output Phase Error
Phase Error (deg)
Time (us)
Frequency Error
Frequency Error (MHz)
Time (us)
Chirp Analysis
Tstart = 61.5us, Tstop = 113us
Set Chirp Rate: 4.8828MHz/us
Results of Linear Regression:
Chirp Rate: 4.8979MHz/us, error: 15.1kHz/us
Freq. Deviation from linear:
RMS: 439kHz Peak: 2.45MHz
Phase Detector Output
PD Out (uA)
Time (us)
Components
FreqDomain
TimeDomain
Schematic
Report

Diseño de la PCB

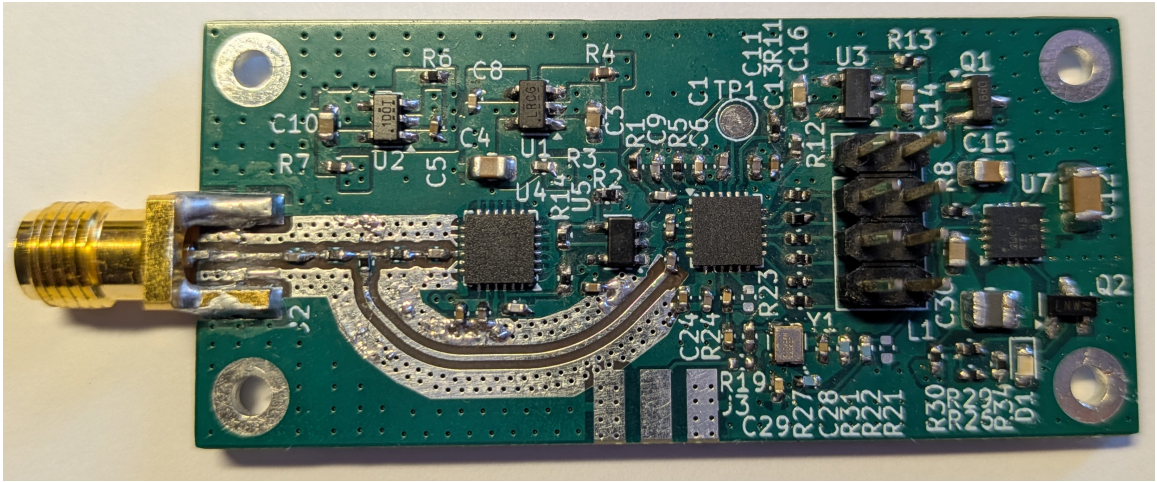
- Diseño inicial en 2 capas, siguiendo stackup recomendado por Alex EA4BFK.
- Rediseño en 4 capas por cuasi unanimidad popular.
- Stackup FR4 controlado en impedancia de JLCPCB.
- CPWG de 0.37 mm de ancho: match razonable para componentes 0402 (ancho 0.5 mm).
- Coste de fabricación: $7.10 por 5 PCBs (coste real con descuentos y envío 3.36€).
- Coste de BOM unos 50-60€.

2) JLC04161H-7628 Stackup

Layer	Material Type	Thickness	
Top Layer	Copper	0.035mm	
Prepreg	7628*1	0.21040mm	
Inner Layer L2	Copper	0.0152mm	1.1mm H/HOZ with copper
Core>	Core	1.065mm	
Inner Layer L3	Copper	0.0152mm	
Prepreg	7628*1	0.21040mm	
Bottom Layer	Copper	0.035mm	

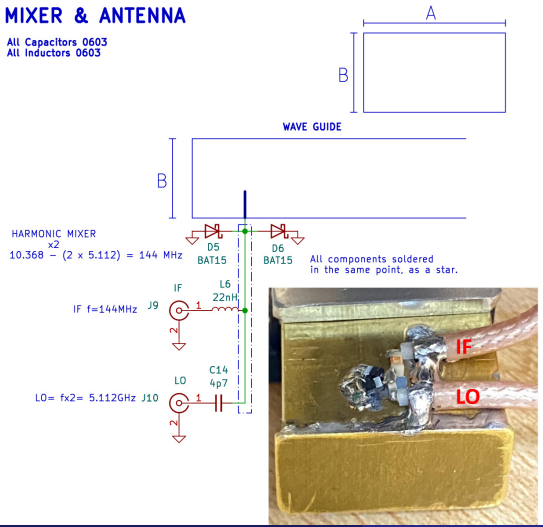


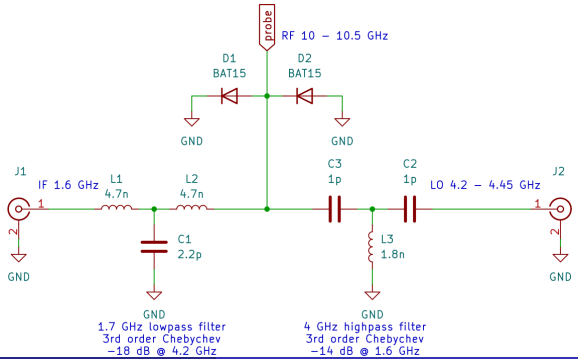
PCB ensamblada a mano



Próximos pasos

- Diseño mezclador armónico: menor ratio IF/LO require mejor filtrado.





Próximos pasos

- Amplificación y distribución LO:
  - El PCB del LO da -1 dBm (supuestamente)
  - Se necesita distribuir el LO a 2 mixers: TX y RX
  - ¿Cuál es la potencia de LO óptima para el mixer?
- ¿Supresión de banda lateral indeseada?
  - El Nestransverter original también transmite/recibe en $2 \times 5.112\ \mathrm{GHz} - 144\ \mathrm{MHz} = 10.08\ \mathrm{GHz}$.
  - El radar FMCW también transmite/recibe en $2 \times [4.2, 4.45]\ \mathrm{GHz} - 1.6\ \mathrm{GHz} = [6.8, 7.3]\ \mathrm{GHz}$.
  - ¿Es el probe y la guía de ondas suficiente atenuación en 7.3 GHz (por ejemplo con WR-75) o se necesita un filtro de 10 GHz en TX?